Shock Performance Study of Solder Joints in Wafer Level Packages

Amarinder Singh Ranouta[1], Xuejun Fan[1, 2], Qiang Han[2]
[1]Department of Mechanical Engineering
Lamar University
PO Box 10028, Beaumont, TX 77710, USA
[2]College of Civil Engineering and Transportation
South China University of Technology, Guangzhou, China
xuejun.fan@lamar.ed/26 2Uue()-5(/U 2Uu)-5 @lamriTUnnamriTUn 0 (out)11.2(h C6

the shock performance of large array wafer level packages. For standard JEDEC drop test, it has been found that corner component group (group A) failed first for 12 12 array packages. This is different from previously reported failure test data of BGA packages. Careful analysis concluded that the high failure rate of group A is mainly due to the effect of

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element modeling using newly developed direct acceleration input method (DAI) is applied. Global/local modeling is adopted to capture both board strains and solder joint stresses accurately. Experimental results are compared to the simulation data. The effects of array size and failure locations are studied in detail. The correlation between board strain and solder joint stress is described. Several new findings through both test and simulation are discussed.

2. Experimental Setup [6]

In this study, a JEDEC test board has been used with dimensions 132mm 77mm 1mm. The test board has 15 copper post wafer level packages with different array sizes. The packages are populated on one side in a three-row, five-column format, as shown in Figure 1.

Figure 1 JEDEC test board and strain gauge rosette attachments

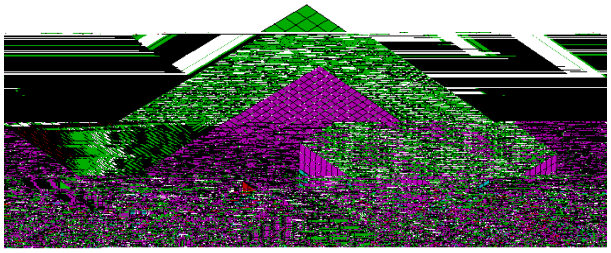
Figure 2 is a schematic view of solder bump structure for a copper post wafer level package. A thick copper post, which is encapsulated by epoxy, is formed on wafer level before ball attachment. The geometric dimensions of the WLP are given in Table 1. The ball pitch is 0.5mm. The test assemblies have been subjected to a 1500g, 0.5ms pulse consistent with the JESD22-B111. The drop height and the pulse shape have been adjusted using pulse shapers between the impacting surfaces. A half-sine pulse has been achieved. Figure 3 shows the schematic of shock test platform, acceleration profile of shock table, and the arrangement of components (face-down) and numbering.

Table 1 Geometrical dimensions of copper post WLP

	Dimensions (μm)
Silicon thickness	400
Solder ball diameter	310
Solder ball standoff height	240

Solder ball opening .479989]0(lder)-50en6] has 15


Y




X

Figure 8 Strain time history comparison for experimental and FEA prediction for U8 in x-direction

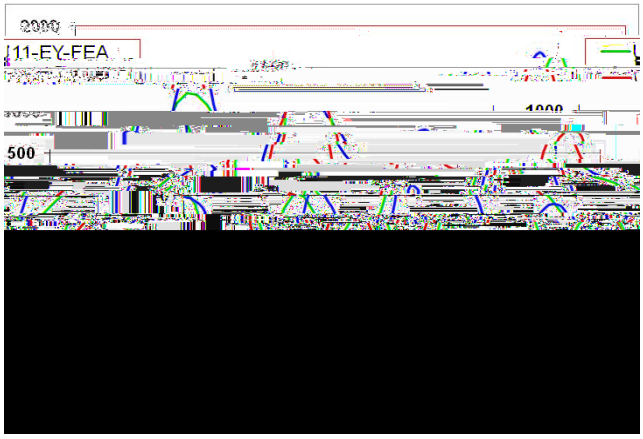


Figure 11 Strain time history comparison for experimental and FEA prediction for U11 in y -direction

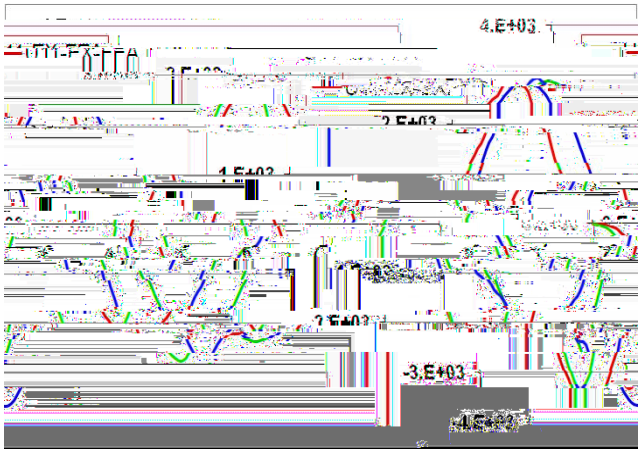


Figure 9 Strain time history comparison for experimental and FEA prediction for U11 in x-direction

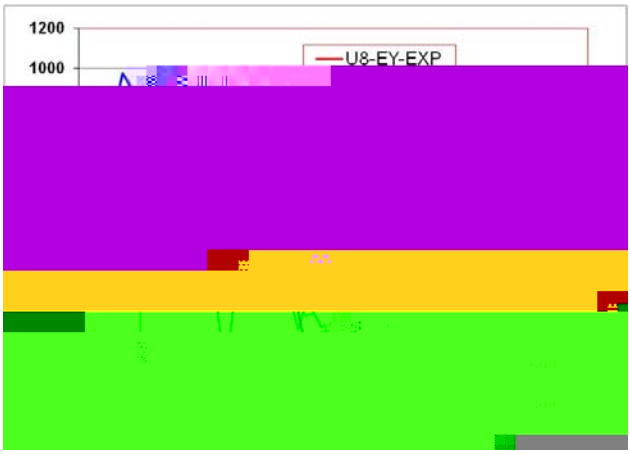


Figure 10 Strain time history comparison for experimental and FEA prediction for U8 in y -direction

Modal analysis is also performed with the global finite element model. The first two symmetrical modes and the corresponding natural frequencies are calculated as 220Hz and 654Hz, respectively from modeling. It is seen that at fundamental frequency, the mode shape is $_x$ dominant. While at 654Hz the mode shape is y dominant. Modeling results correlate very well with measured data in Figure 5 (230Hz and 650Hz).

5 Board Strains An8 t5 Boar

5.2 Effect of Array Size

In previous section, it is discovered that U1 has maximum board corner strain. Here its behavior has been tested for different array sizes. Figure 17 plots the maximum principal strain and maximum x-strain at U1 in array sizes from 6×6 to

28×28. As array size increases beyond 20×20 (package size 10mmx10mm), strain decreases in PCB board. This nature is found not only with maximum principal strain but the same as with strain in x-direction.

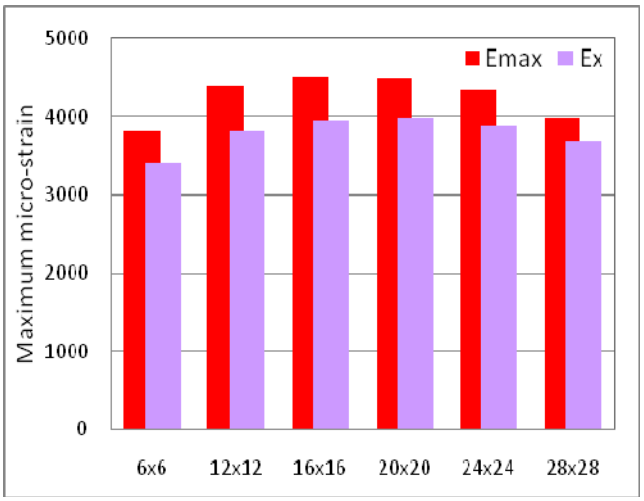


Figure 17 Plot for maximum principal strains and strains in X-direction at U1 of different arrays

Now let us look at behavior of strains induced at U3 and U8 components with different array sizes in JEDEC board, as shown in Figure 18 and 19. It clearly shows the fact that with increase in array size, both principal strains and strains induced in x-direction at component U3 and U8 increase.

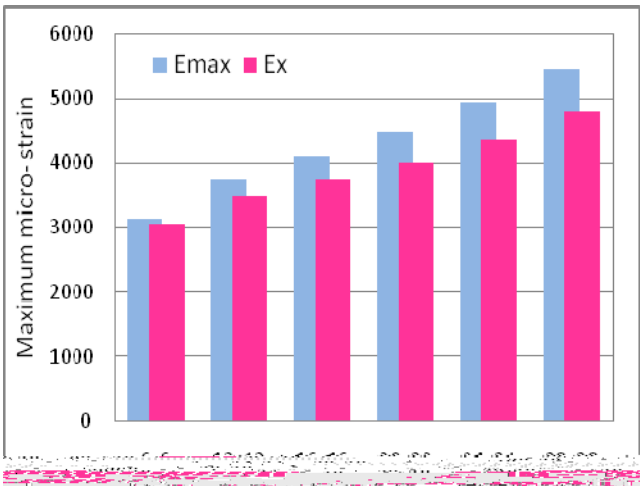


Figure 18 Plot for maximum principal strains and strains in x-direction at U3 of different arrays

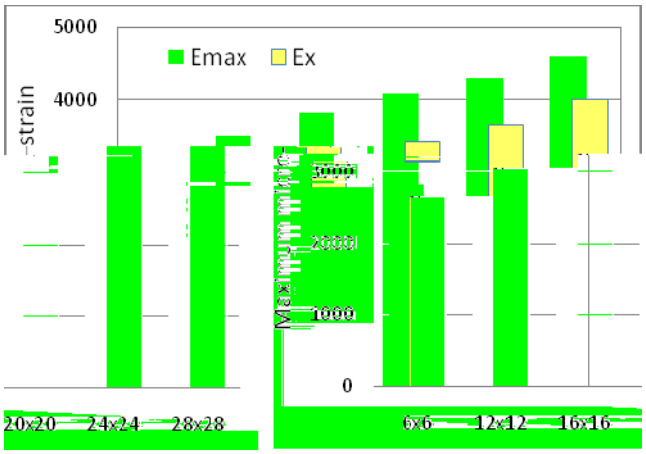


Figure 19 Plot for maximum principal strains and strains in x-direction at U8 of different arrays

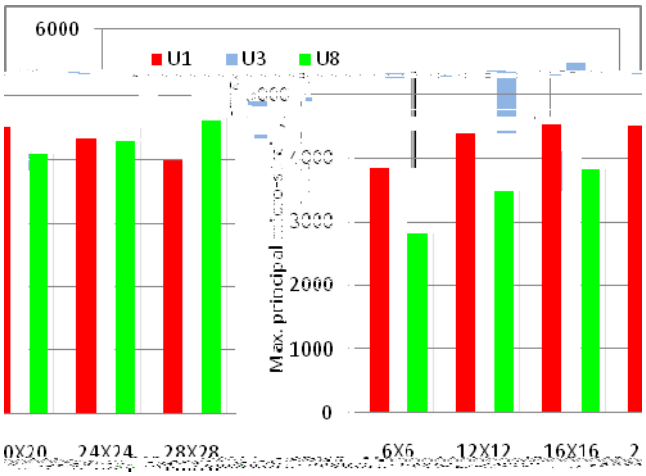


Figure 20 Plot for comparison between maximum principal strains induced at U1, U3 & U8 of different arrays

Figure 20 plots the compiled strain data for components U1, U3 and U8 for different array sizes. From this figure U1, U3 and U8 are ranked for various array sizes as shown in Table 3. It can be seen that the rank changes with array size. This implies that with large array size, the first failure may shift from the component U1 to U3 and U8.

Table 3 Ranking of U1, U3 and U8 based on maximum principal strain with different sizes

Array Size	Rank
6x6	U1 > U3 > U8
12x12	U1 > U3 > U8
16x16	U1 > U3 > U8
20x20	U1 > U3 > U8
24x24	U3 > U1 > U8
28x28	U3 > U8 > U1

6. Strain Comparison between Global and Local Models

To check whether global/local model built is accurate or not, corner strains from global model and local model with

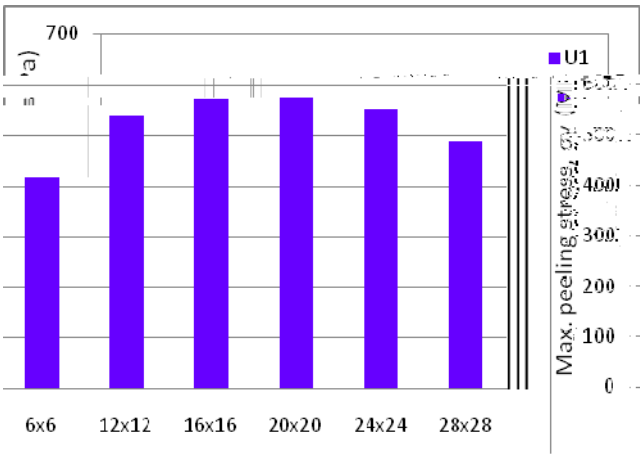


Figure 25 Plot for maximum peeling stresses at U1 of different array sized WLPs

Figure 26 and Figure 27 are the patterns of maximum

Novel finite element modeling approach has been

"A Methodology for Droop Performance Prediction and Application for Design Optimization of Chip Scale Packages," *2005 Electronic Components and Technology Conference*.

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